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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/706,752	11/07/2000	Ramesh Padmanabhan	0023-0001	5989

26615 7590 11/18/2003

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EXAMINER	
WANG, ALBERT C	
ART UNIT	**PAPER NUMBER**
2185	2

DATE MAILED: 11/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/706,752	PADMANABHAN ET AL.	
	Examiner	Art Unit	
	Albert Wang	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Original claims 1-44 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4-9, 15-22 28-32, 36-40, and 44 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang, U.S. Patent No. 5,563,891.

As per claim 1, Wang discloses a system for reliably receiving data, comprising:

a memory (Fig. 3, elastic buffer 620);

write logic configured to receive data and an unreliable clock signal and write the data to the memory using the unreliable clock signal (Fig. 3, write data of lower rate signal to elastic buffer using recovered write clock; Col. 2, lines 10-21, clock from lower rate signal is unreliable); and

read logic configured to generate a gapped clock signal and read the data from the memory using the gapped clock signal, the gapped clock being generated by turning on and off a constant local clock signal (Fig. 3, gapped read clock generated from local oscillator 640).

As per claim 4, Wang discloses the read logic includes a gapped clock generator configured to generate the gapped clock signal from the constant local clock signal (Col. 2, lines 46-52, gapped read clock).

As per claim 5, Wang discloses the gapped clock generator includes:

a first state machine generate an enable signal having at least two states (Fig. 3, justification decision circuit 635; Fig. 4c, justification signal has high and low states; Col. 3, lines 62-65, justification signal acts as enable signal);

a second state machine configured to turn on and off the constant local clock signal based on the state of the enable signal to generate the gapped clock signal (Fig. 3, logic circuit 645; Col. 3, lines 53-57).

As per claim 6, Wang discloses the read logic further includes a component configured to determine whether the memory contains data (Fig. 3, comparison circuit 630).

As per claim 7, Wang discloses the component includes a comparator configured to determine whether the memory contains data by comparing a write address used by the write logic to access the memory to a read address used by the read logic to access the memory (Col. 3, lines 26-29).

As per claim 8, Wang discloses the second state machine is configured to turn off the constant local clock signal when the memory contains no data (Col. 3, lines 39-52, when memory level is below a threshold, justification signal is low; Col. 3, lines 62-65, when justification signal is low, read clock is not enabled).

As per claim 9, Wang discloses the unreliable clock signal operates at a frequency lower than a frequency of the constant local clock signal (Col. 2, line 65-67, "the read clock is faster than the write clock"); and

wherein the read logic is configured to compensate for underflow conditions in the memory by turning off the constant local clock signal (Col. 4, lines 23-27, reduce or eliminate

slips; Col. 3, lines 39-52, when memory level is below a threshold, justification signal is low; Col. 3, lines 62-65, when justification signal is low, read clock is not enabled).

As per claim 15, Wang discloses a system for reliably receiving data, comprising:

means for receiving data and an unreliable clock signal (Fig. 3, data of lower rate signal and recovered write clock; Col. 2, lines 10-21, clock from lower rate signal is unreliable);

means for writing the data to a memory using the unreliable clock signal (Fig. 3, writing to elastic buffer 620);

means for generating a gapped clock signal to compensate for underflow conditions in the memory (Fig. 3, gapped read clock; Col. 4, lines 23-27, reduce or eliminate slips); and

means for reading the data from the memory using the gapped clock signal (Fig. 3, read-out of data of lower rate signal using gapped read clock).

As per claims 16-22, since Wang discloses the system of claims 1 and 4-9, Wang discloses the claimed method.

As per claim 28, Wang discloses a receiver, comprising:

a receiver component (Fig. 3, desynchronizer 70); and

a reliable clock generator configured to receive data and an unreliable clock signal (Fig. 3, write data of lower rate signal to elastic buffer using recovered write clock; Col. 2, lines 10-21, clock from lower rate signal is unreliable), generate a reliable clock signal to compensate for underflow conditions in the memory (Col. 4, lines 23-27, reduce or eliminate slips), read the data from the memory using the reliable clock signal (Fig. 3, read-out of data of lower rate signal using gapped read clock), and provide the data and the reliable clock signal to the receiver component (Fig. 3, provide higher rate signal to desynchronizer).

As per claims 29-32 and 36, since Wang discloses both the system of claims 4-9 and the receiver of claim 28, Wang discloses the claimed receiver.

As per claim 37, Wang discloses a clock generator, comprising:

a first state machine configured to generate first and second enable signals (Fig. 3, frame timing and justification signal), the first enable signal being used to read data from a memory that was written to the memory using an unreliable clock signal (Fig. 3, read-out of data of lower rate signal from elastic buffer 620; Col. 2, lines 10-21, clock from lower rate signal is unreliable); and

a second state machine configured to generate a gapped clock signal for reliably recovering the data in response to the second enable signal (Fig. 3, logic circuit 645; Col. 3, lines 53-65, justification signal acts as enable signal).

As per claims 38-40 and 44, since Wang discloses both the system of claims 4-9 and the clock generator of claim 37, Wang discloses the claimed clock generator.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2, 3, 10, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang as applied to claim 1 above, and further in view of Co et al., U.S. Patent No. 5,602,882 ("Co").

As per claim 2, Wang teaches the write logic includes a write pointer configured to generate an address for writing the data into the memory (Fig. 3, write pointer 115; Col. 2, lines 35-46). Wang does not expressly teach the details of a register to buffer the data. Such a register is well known in the art. Co teaches such a register (Fig. 3, receive buffer 22). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Co's register to Wang's system in order to ensure the integrity of the system.

As per claim 3, Co teaches the memory includes a first-in first-out memory (Abstract, FIFO).

As per claim 10, Wang teaches teaches the unreliable clock signal operates at a frequency higher than a frequency of the constant local clock signal (Col. 3, lines 1-5, "read clock is slower than the write clock"). Co teaches generating a data error when overflow conditions occur (Col. 2, lines 33-38).

As per claim 23 since, Wang/Co teaches the system of claims 1 and 10 and the method of claim 16, Wang/Co teaches the claimed method.

4. Claims 11-14, 24-27, 33-35, and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang as applied to claims 1, 16, 32 and 40 above, and further in view of Mays et al., U.S. Patent No. 5,384,770 ("Mays").

As per claim 11, Wang teaches the read logic is configured to turn off the constant local clock signal when the write logic receives no unreliable clock signal (Fig. 4, when phase difference is below the threshold, justification signal is low, so that read clock is not enabled), but does not expressly teach starting a counter. Mays teaches starting a counter when no data is received (Col. 11, lines 37-51, timer 17 counts down when no character interrupt signal is

received). In Wang when no data is received, no unreliable clock signal is recovered. At the time of the invention, it would have been obvious to one skilled in the art to apply Mays' starting a time-out counter to Wang's system. A motivation for doing so would have been to limit delays due to waiting for data accumulation (Col. 4, lines 20-33).

As per claim 12, Mays teaches determining write logic has received data before the counter reaches a predetermined count (Col. 11, lines 37-51, character interrupt signal is received before timer 17 reaches zero).

As per claims 13 and 14, Mays teaches determining that the counter has reached a predetermined count (Col. 11, lines 37-51, "timer 17 counts down from a predetermined initial value to zero and produces a time-out signal").

As per claims 24-27, since Wang/Mays teaches the system of claims 11-14 and the method of claim 16, Wang/Mays teaches the claimed method.

As per claims 33-35 since Wang/Mays teaches the system of claims 11-14 and the receiver of claim 32, Wang/Mays teaches the claimed method.

As per claims 41-43 since Wang/Mays teaches the system of claims 11-14 and the clock generator of claim 40, Wang/Mays teaches the claimed clock generator.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

aw
November 3, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
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